
# AL8243 Core
# Application Note

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# General Information

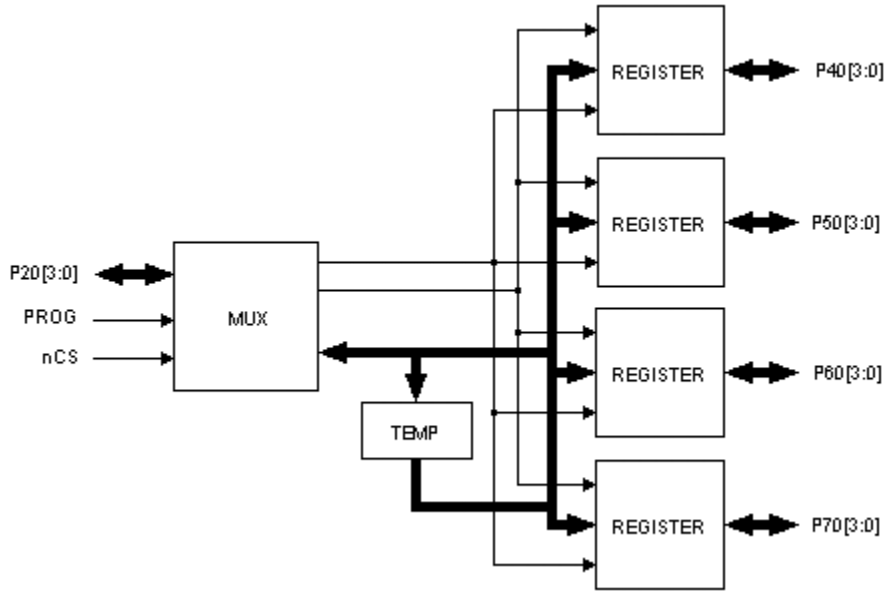
The AL8243 core is the VHDL model of the Intel™ 8243 input/output expander.

# Features

- Functionally based on the Intel 8243 device
- Five 4-bit peripheral ports: P20, P40, P50, P60, P70
- Two control signals: CS, PROG
- Four programming modes for peripherals (three write and read modes)
- 4-bit bidirectional system data bus with standard microprocessor interface controls

# Block Diagram

The basic structure of the AL8243 core is shown below:



# Contents

## Behavioral

The behavioral model is designed for the functional simulation only and it cannot be synthesized or implemented into FPGAs. The behavioral model contains the following files:

- **AL8243.vhd** – the top level file of the AL8243 model

## Synthesizable

See the Deliverables section of this document for further details.

## Test Vectors

See the Deliverables section of this document for further details.

# Interface

The pinout of the AL8243 core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in the table.

| Signal Name | Signal Direction | Polarity | Description |
|---|---|---|---|
| PROG | IN | - | CLOCK INPUT. A high-to-low transition on the PROG input signifies that the address and control bits are available on the P20 port, and a low-to-high transition signifies that data are available on the P20 port. |
| nCS | IN | LOW | CHIP SELECT INPUT. A high on the CS input inhibits any changes of the output signals or the internal status. |
| P20[3:0] 1) | INOUT | - | 4-bit bidirectional port contains the address and control bits on a high-to-low transition of the PROG input. During a low-to-high transition, the port contains data for a selected output port during the write operation, or the data from a selected port before the low-to-high transition during the read operation. |
| P40[3:0] 1)<br>P50[3:0]<br>P60[3:0]<br>P70[3:0] | INOUT | - | 4-bit bidirectional I/O ports. Could be programmed as the input (during the read operation), low impedance latched output (after the write operstion), or the tri-state (after the read operation). Data on pins P20-P23 could be written directly or logically mixed with previous data (AND or OR logic). |

**NOTES:**

1. Each bidirectional pin is defined in the core interface as three separated VHDL ports. Optionally, using the VHDL Interface (See the Deliverables section of this document for further details), it can be merged to one bidirectional VHDL port.

# Implementation Data

The core has been synthesized and implemented to different types of reprogrammable devices. The model has been verified using the simulation environment and tested on the real hardware.

| Software | | | | |
|---|---|---|---|---|
| Synthesis Tool | Synopsys FPGA Express™ build 2.1.3.3220 | | | |
| Implementation Tools | Xilinx Foundation™ 2.1i SP2, Altera MAX+plusII™ 9.21, Quartus™ 1.0 A | | | |
| Verification Tool | Active-HDL™ 3.5 build 437 | | | |
| **Hardware** | | | | |
| Vendor | Xilinx | | Altera | |
| Device Family | 4K | Virtex™ | FLEX™ 10K | APEX™ 20K |
| Target Device | XC4062XLA-9 | XCV300-4 | EPF10K100-1 | APEX20 |
| Area | 37CLBs (1%) | soon come | soon come | soon come |
| System Clock fmax | 54MHz | soon come | soon come | soon come |

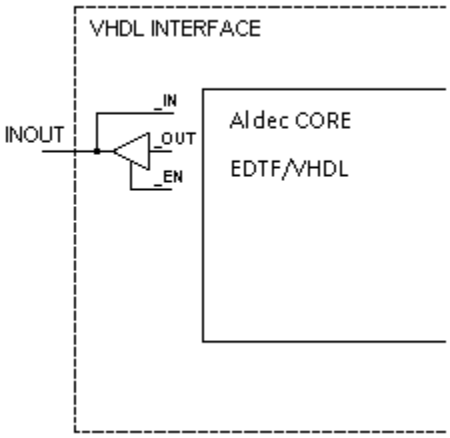
# Deliverables

After you request the desired compiled synthesizable core, Aldec delivers the following files:

- Both technology-dependent EDIF (AL8243_CORE.EDN) and VHDL (AL8243_CORE.VHD) netlists
- Aldec VHDL Interface (AL8243.VHD)
- User-Guide and Application Notes
- Sample designs

Usually Aldec delivers both EDIF and VHDL netlists for customers who order the synthesizable model. The EDIF netlist is used for the place and route process and VHDL is the post-synthesis netlist used for the simulation only. Of course, both netlists are technology-dependent, because they are created after the synthesis where the customer needs to specify a vendor, target family, etc.

Aldec provides optionally a VHDL interface for its synthesizable models for these customers who need bidirectional ports in the core interface. See the picture below:




Aldec provides also a set of VHDL test benches for their cores. Usually they are sold at the additional charge.

Source codes are sold on a case-by-case basis.